REMARKS

The application has been amended to place the application in condition for allowance at the time of the next Official Action.

Claims 1-6 were previously pending in the application. Claims 3-6 are canceled, leaving claims 1 and 2 for consideration.

Claims 1-3 and 5 are rejected as anticipated by ZASIO et al. 4,495,629. This rejection is respectfully traversed.

Claim 1 provides a first scan controller for receiving an output signal from a master latch and outputting received output signal in synchronism with a scan clock. Claim 1 further provides a second scan controller having an input terminal connected to an output terminal of the first scan controller. The second scan controller is in synchronism with the scan clock when the semiconductor integrated circuit device is tested.

ZASIO et al. disclose a scanning flip-flop circuit which is equipped with first, second and third latch elements. When the scanning flip-flop circuit operates as a latch circuit, the first and second latch elements operate as a master/slave circuit, wherein the master includes transmission gates T1 and T2 and the slave includes transmission gates T3 and T4. When the scanning flip-flop circuit operates as a shift register, the second and third latch elements operate as a master/slave circuit

and perform the shift action of data with the clock signal, wherein transmission gates T1 and T2 are the master section and transmission gates T7 and T8 are a separate slave section as disclosed on column 6, lines 19-32 in conjunction with Figure 3 of ZASIO et al. By having the separate scan section, ZASIO et al. is able to monitor the circuit more readily.

In contrast, the present invention sets forth a circuit which realizes improvement in the speed of the scanning flip-flop circuit, without adding a special circuit for making an examination. By not adding a circuit for making an examination, the present invention also has the effect of not increasing the circuit size or power consumption of a semiconductor integrated circuit.

With the growth of multi-functionalism and multiple applications for integrated semiconductor circuits, high density design and power-saving capabilities in integrated semiconductor circuits have become important in recent years.

Further, the Official Action has indicated that the inclusion of the first scan controller is merely a design choice and does not effect the operation of the master/slave circuit during either normal or scan operation. Accordingly, the Official Action has indicated that one of ordinary skill in the art would be able to design a circuit including a first scan

controller (wherein the first scan controller is transparent during the scan mode).

However, the present invention proposes a circuit connection which realizes an improvement in the speed of the master/slave type scanning flip-flip that is provided with a clock controller, a first scan controller and a second scan controller. Without an element that is equivalent to the first scan controller, the circuit composition of ZASIO et al. (Figure 3) is completely different from that of the present invention. Therefore, not having the first scan controller would not be a mere design choice.

It has been held that a finding of "obvious design choice" is precluded where claim structure and the function it performs are different from those of prior art. *In re Chu*, 66 F.3d 292, 36 USPQ2d 1089, 1094, 1095 (Fed. Cir. 1995).

As noted in the Official Action, ZASIO et al. do not teach or suggest the first scan controller. Therefore, ZASIO et al. could not teach or suggest the function of receiving an output signal from a master latch and outputting the received output signal in synchronism with a scan clock as recited in claim 1. Since the structure of the first scan controller recited in claim 1 is absent from ZASIO et al., the function that such scan controller performs is necessarily absent and thus

different from that of ZASIO et al. Accordingly, obvious design choice is precluded.

Claim 2 depends from claim 1 and further defines the invention and is also believed patentable over ZASIO et al.

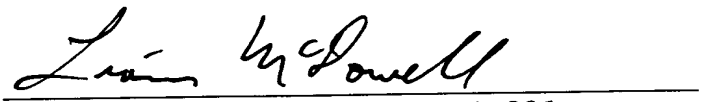
Claims 4 and 6 are rejected as unpatentable over ZASIO et al. This rejection is believed moot since claims 4 and 6 are canceled.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R.§1.17.

Respectfully submitted,

YOUNG & THOMPSON



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